Rad-hard Standard Cells Design in 28nm TSMC

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Effects of HEPs

The main aspect of integrated circuits to be used for space applications is the resistance to radiation. Outside earth (meaning in electronic equipment for satellites, probes or spacecrafts) many particles (electrons, protons, high energy ions) collide with silicon devices releasing energy and affecting working operations.

There are two main effects of radiations on silicon devices:

1. Total Ionizing Dose (TID);
2. Single Event Effect (SEE).

Total Ionizing Dose gives a progressive degradation of the devices thus taking the chip to a general malfunction after months or years.

Single Event Effects is strongly dependent on the amount (and nature) of energized particles and in the worst case can be destructive (SEL, Single Event Latch-up).

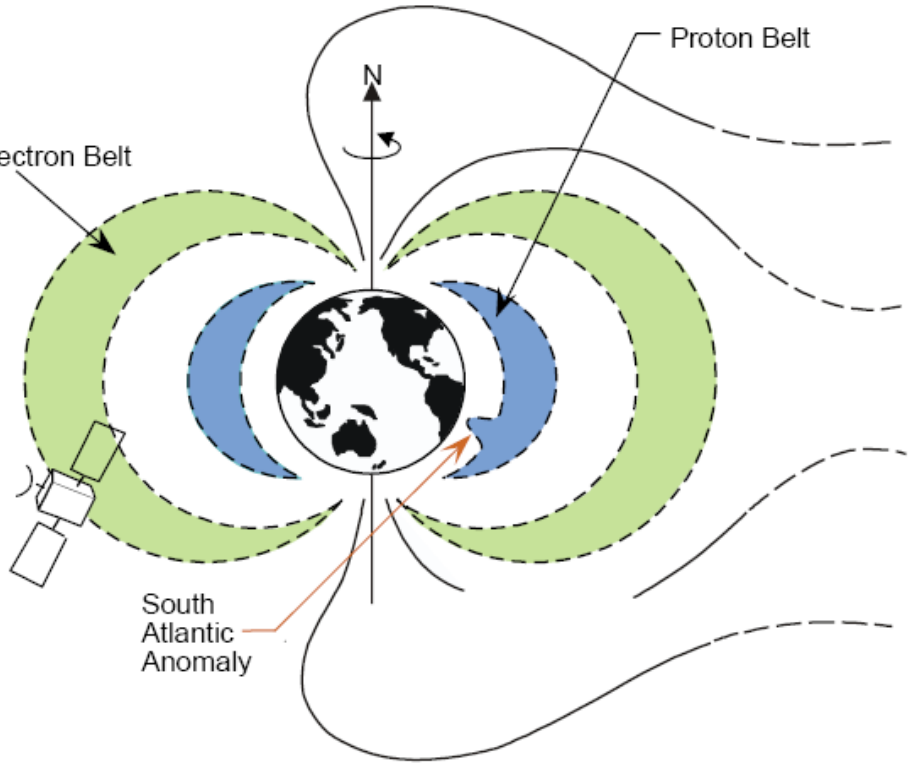
Radiation Environment

Single Event Effects are mainly due to:

1. Galactic cosmic rays (85% protons and 25% heavy ions [1])
2. Cosmic solar particles (heavy ions and protons produced by solar flares)
3. Protons trapped in radiation belts

Cumulative Effects are mainly due to:

1. Protons trapped in radiation belts
2. Electrons trapped in radiation belts
3. Protons from solar flares

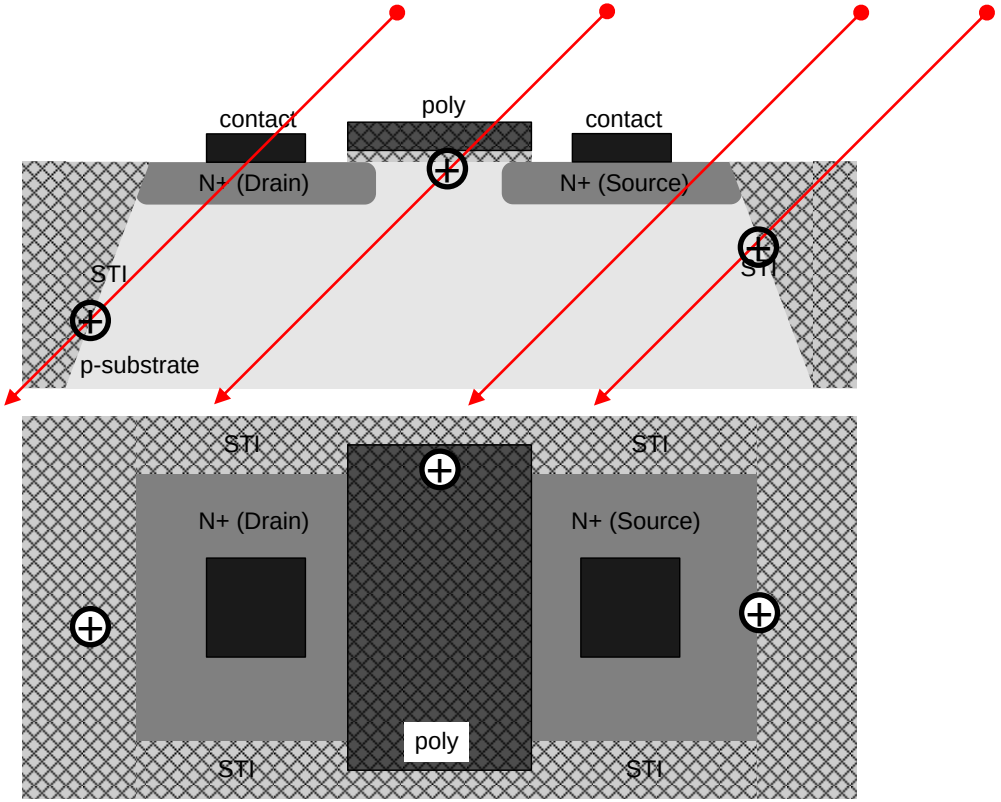


"Space Radiation Effects on Microelectronics" NASA JPL

J. Srour and J. McGarrity,"Radiation Effects on Microelectronics in Space", Proc. Of the IEEE, vol 76 n 11 Nov 1988 pp 1443-1469

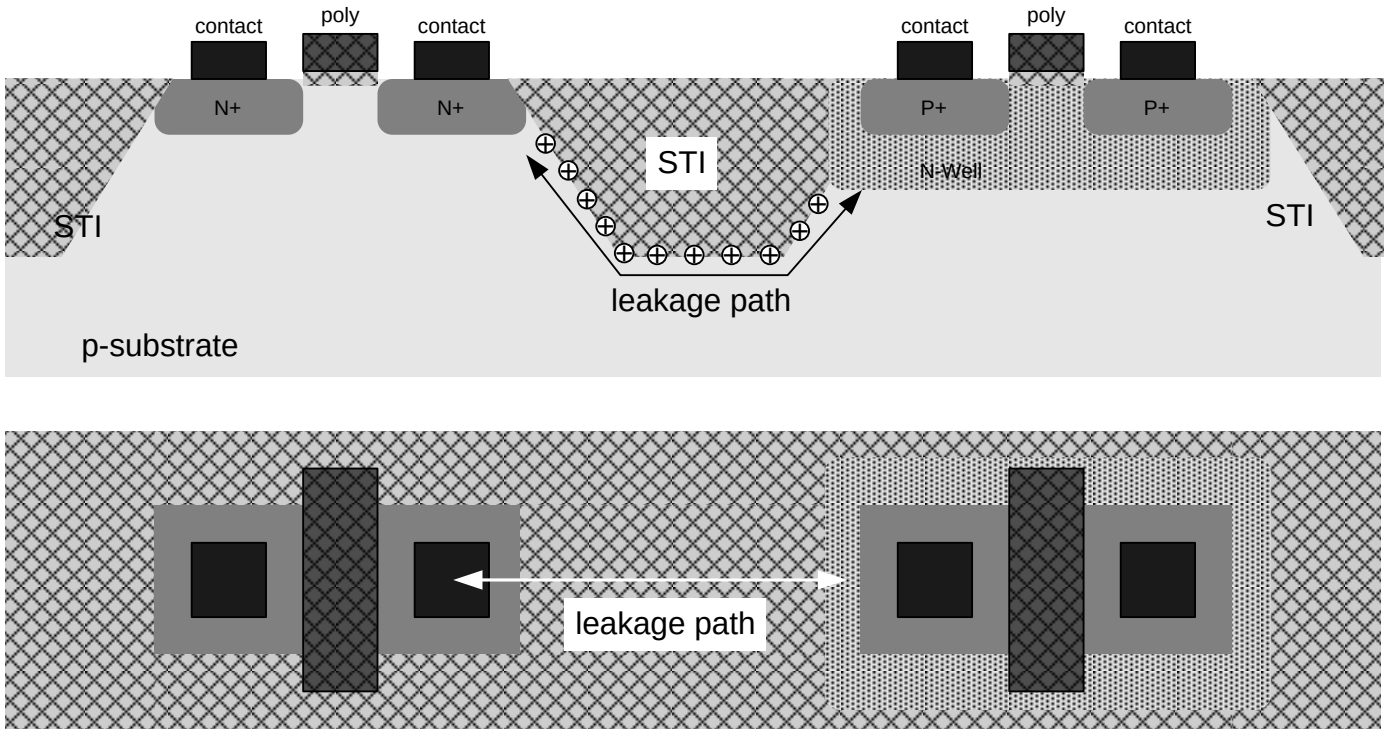
HEPs generation at transistor level

Charged particles hit MOS transistor in all directions and HEPs are generated; In oxides (STI and thin gate oxide) holes can be trapped. The effect is expected to be minimal in the channel for 28nm process. Intra-device leakage should not be a problem.



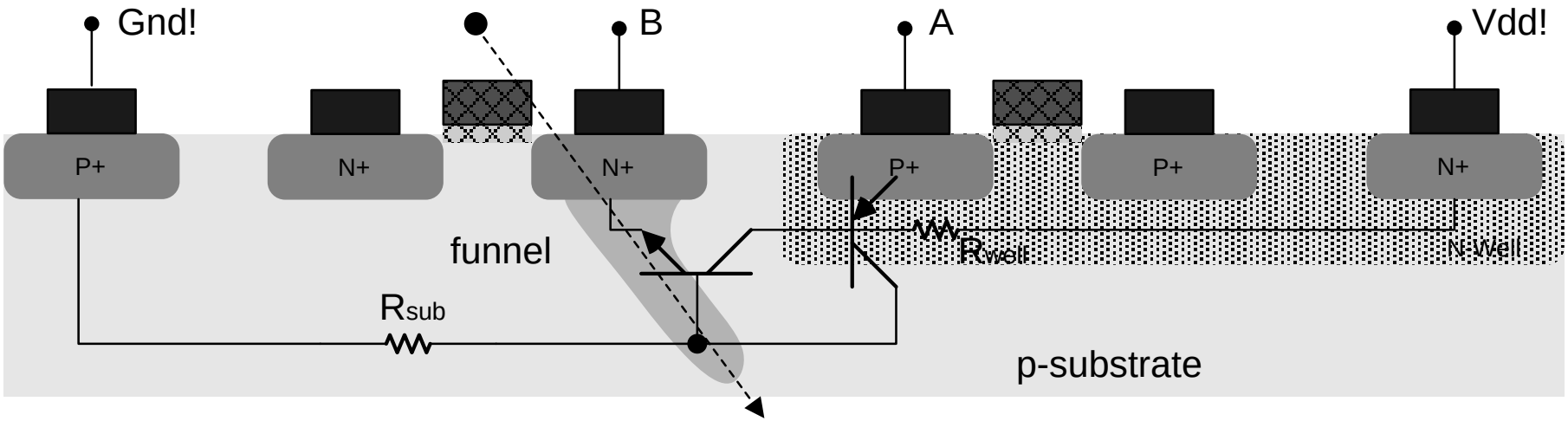
Inter Device Leakage

Inter device leakage occurs between different transistors supposed to be insulated each to the other (N-MOS vs N-MOS or N-MOS vs N-WELL). Inter device leakage may be critical in analog design (e.g. ADC, Op-Amp, etc…). Inter-device leakage must be considered.



Single Event Effects: Hard Errors

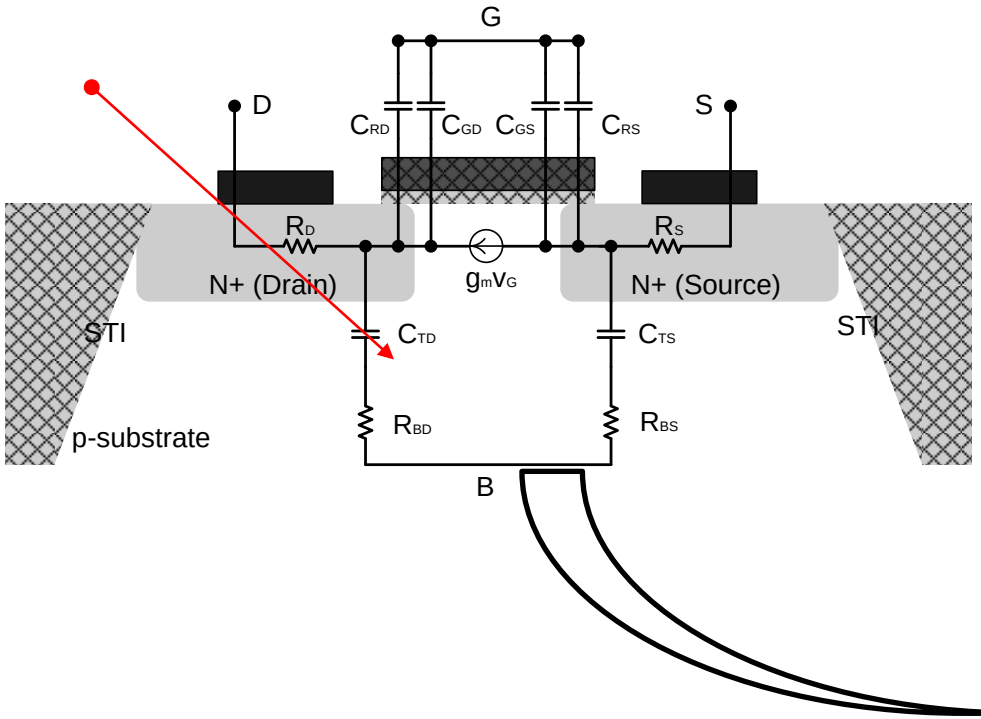
These effects are due to the interaction between a single particle (e.g. heavy ion) and silicon. If the released energy (LET, Linear Energy Transfer) is sufficiently high a latch-up may occur in CMOS structures (SEL, Single Event Latch-up) or a gate may be broken (SEGR, Single Event Gate Rupture). SEL mitigation must be considered in 28nm process.

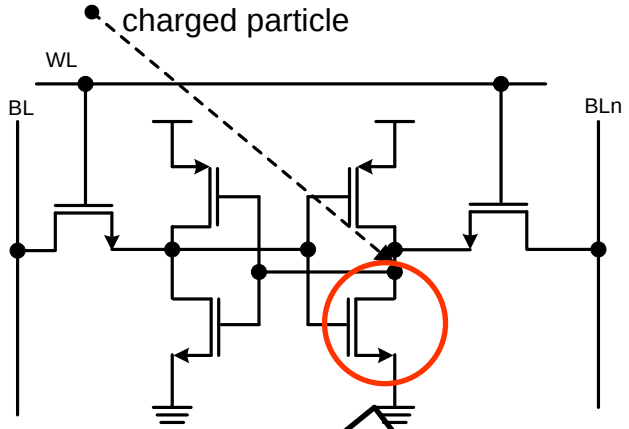


Single Event Effects: Soft Errors (SEU)

SEU (Single Event Upset) has been observed for the first time in 1979 in bipolar Flip-Flops. Actually SEUs are the worst soft errors because of scaling down of silicon processes:

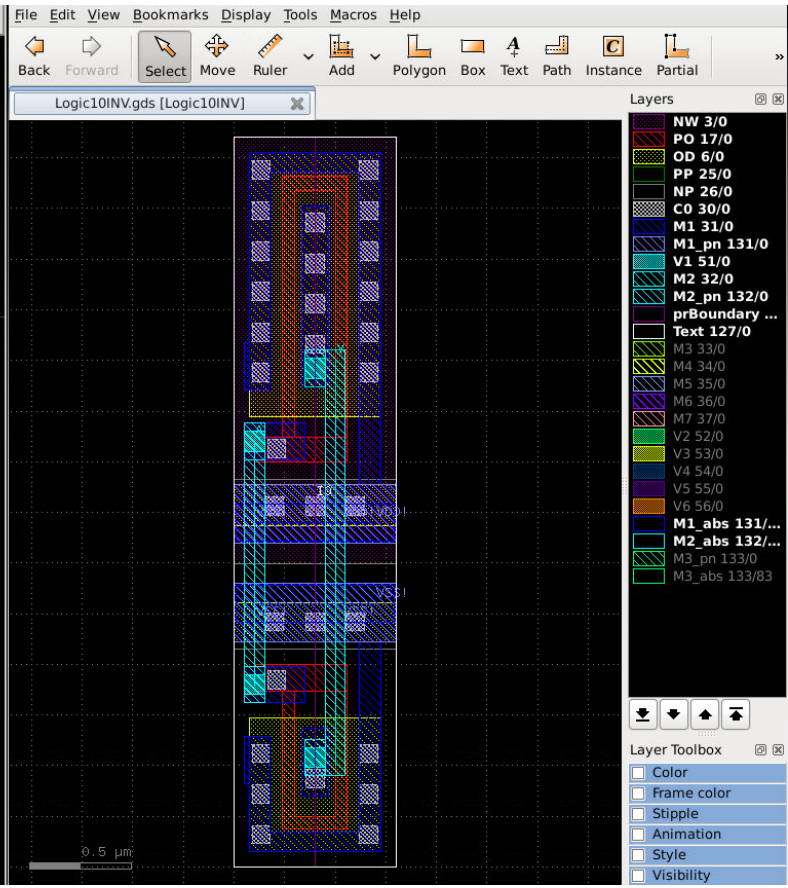
1. Lower “Critical Charge” for submicron technologies;
2. Large number of transistors and increased complexity.





Standard cell base line: RadLibN65GP

The base line for RadLibN28 standard cell library is represented by the already existing RadLibN65GP (TSMC 65nm General Purpose).
RadLibN28 is under development and will not consider ELTs.



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RadLibN28

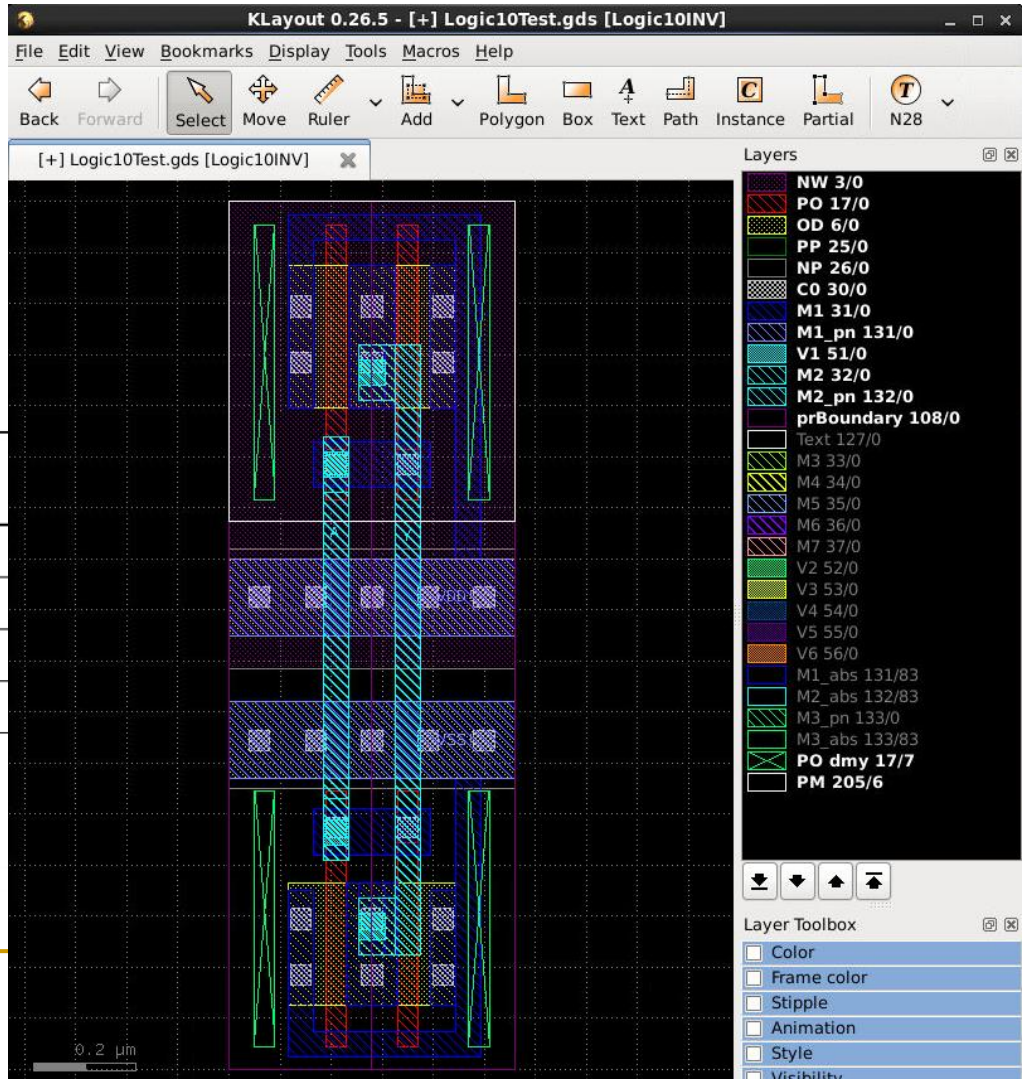
Starting from already existing standard cell libraries in N28 the goal is to shape radiation hardened standard cells keeping the compatibility in terms of grid and power rails.

Table 1.1 Physical Design Specifications

(1) Core and coarse grain cell

Design Dimension	Physical Dimension
Drawn Gate Length	0.035
Vertical Pin Grid	0.1
Horizontal Pin Grid	0.140
Cell Power & Ground Rail Width	0.15

TCBN28HPCPLUSBWP12T30P140 Datasheet



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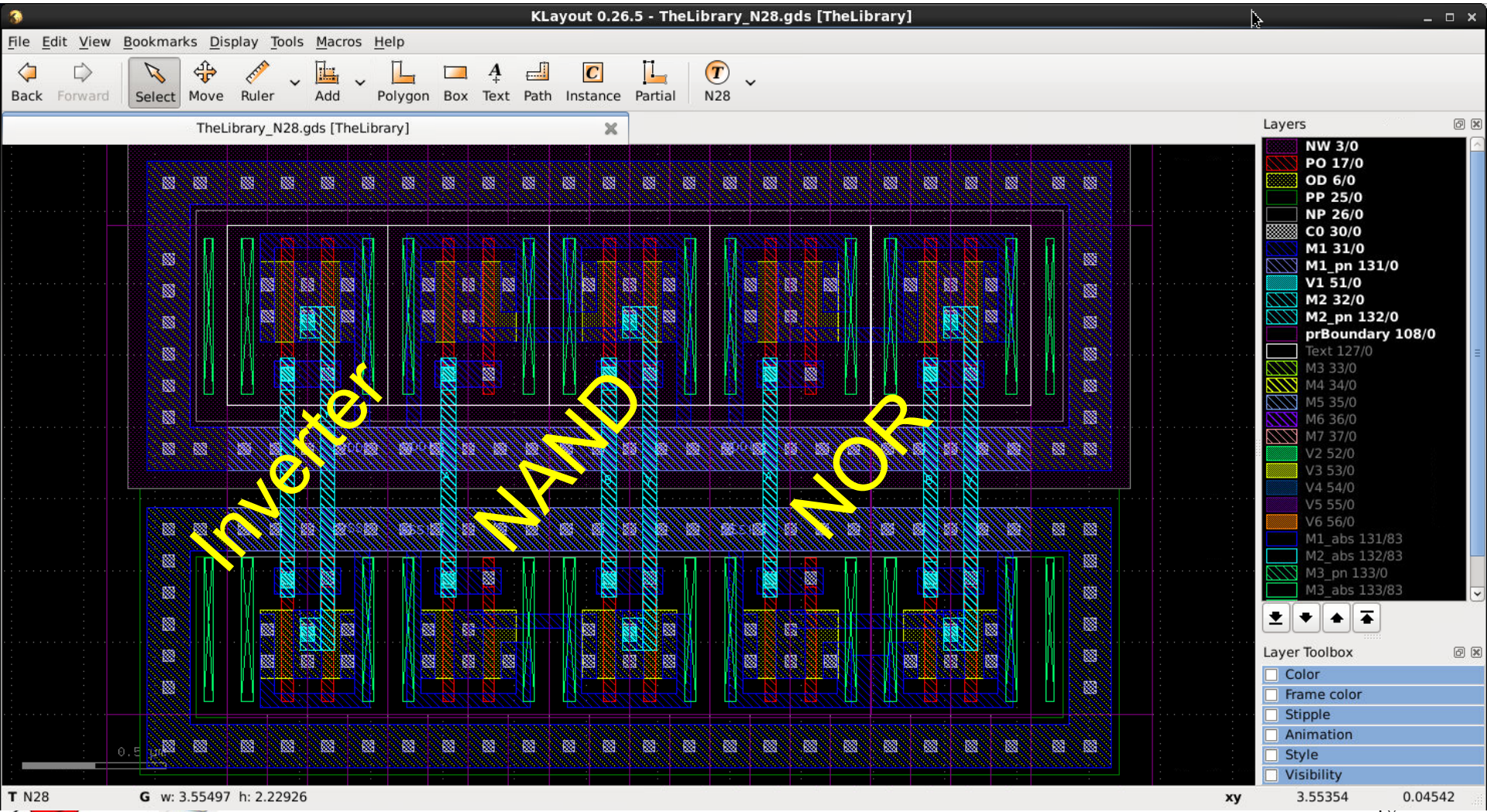
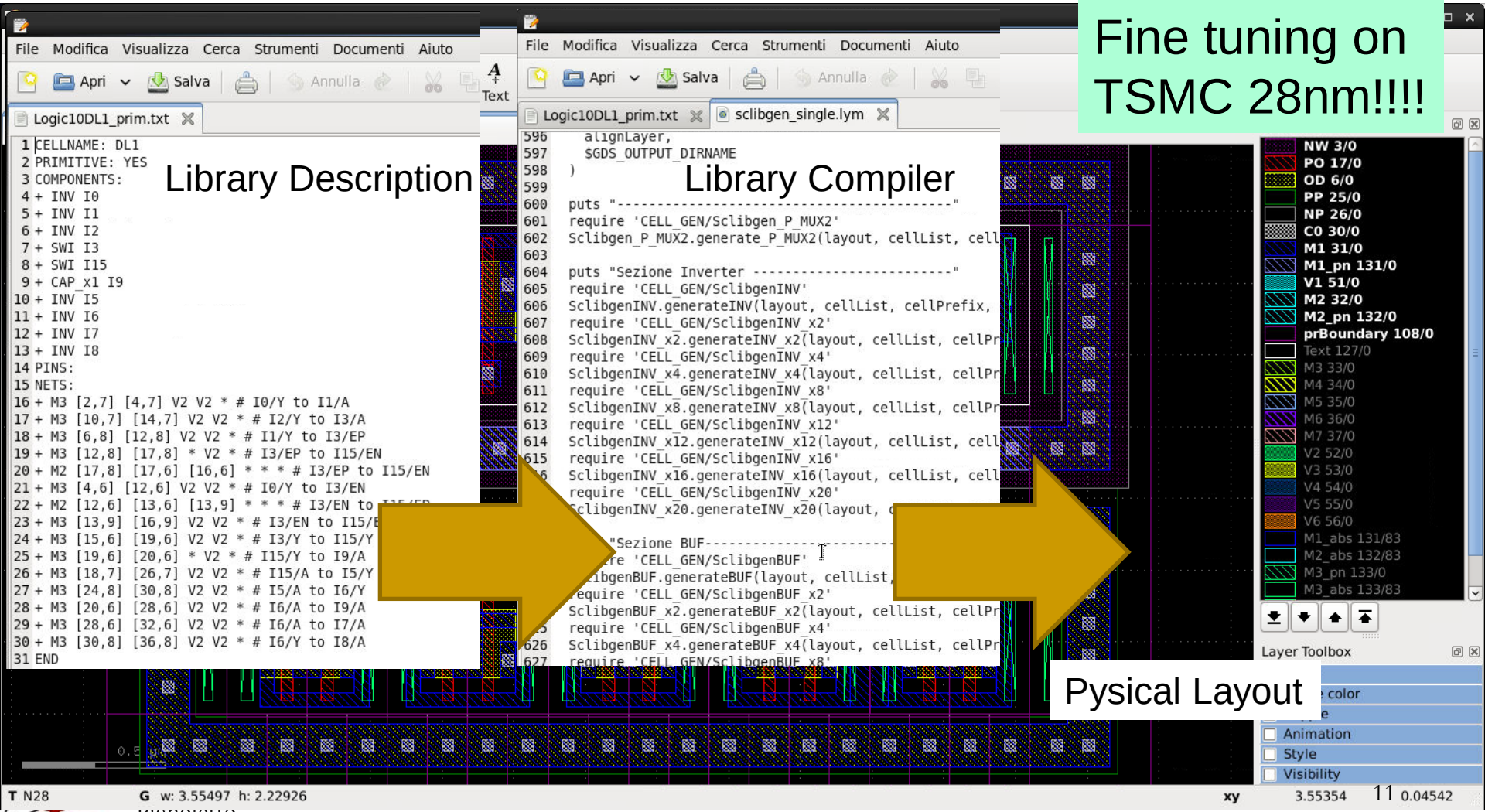
Fully digital approach

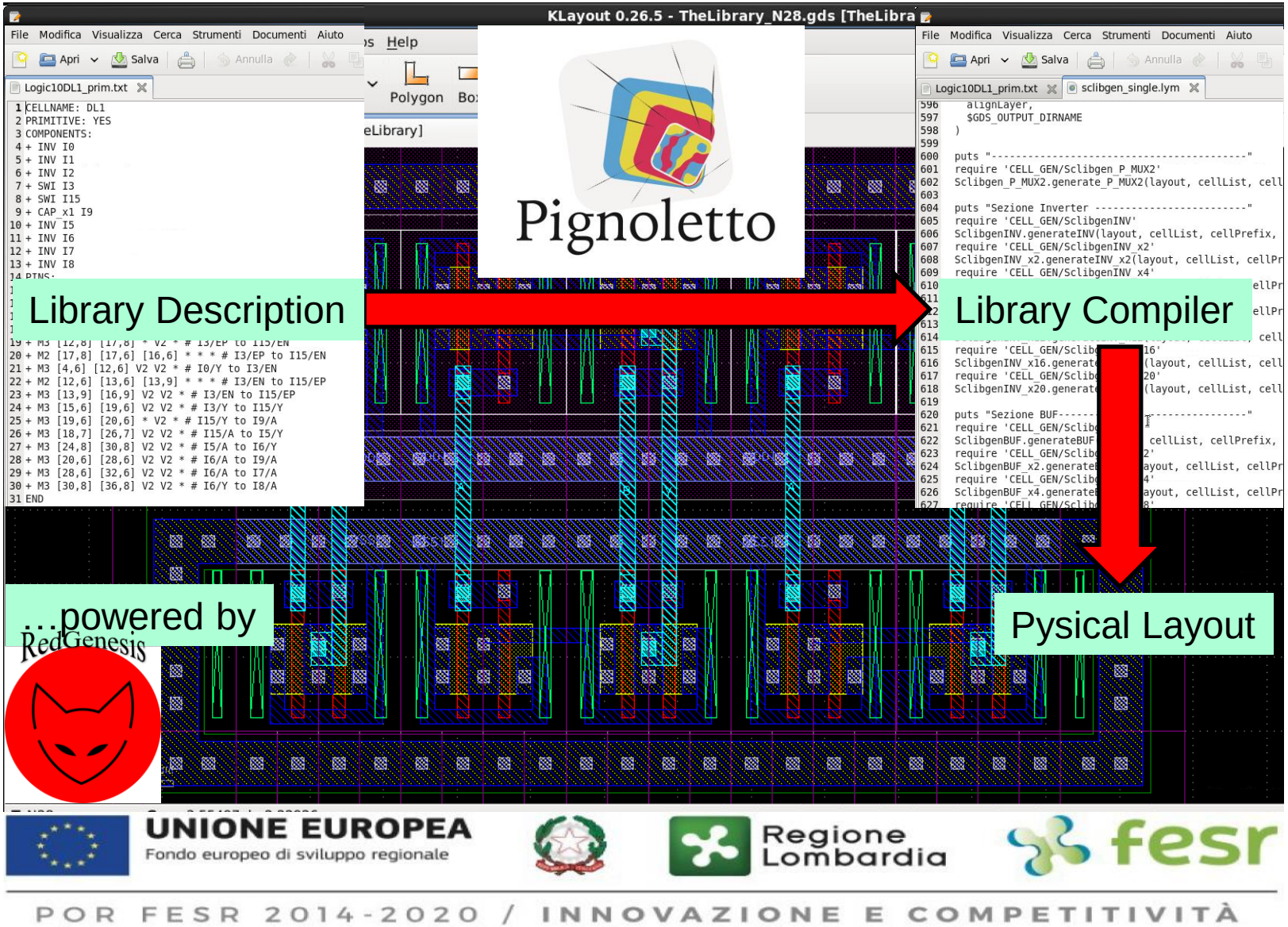
Each standard cell must be shaped to fit P&R requirements in a standard CMOS digital flow (from verilog to GDSII).



Key blocks for standard cell compiler

Starting from a limited set of standard cells (inverter, nand, nor) and closing elements the full library will be compiled using RedGenesis internal tool.





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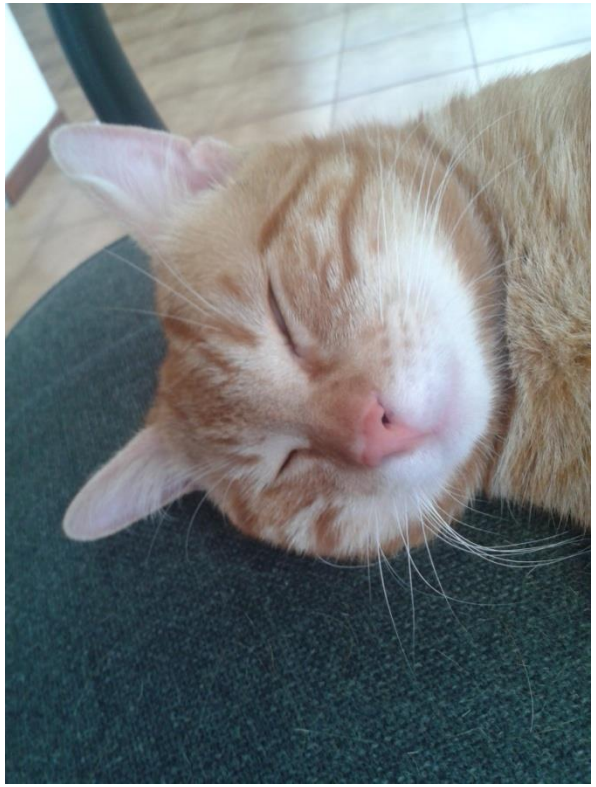
Thanks for your Attention!!



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